of said plurality of main word lines being allotted to one of said plurality of sets of sub-word lines;

a plurality of second regions, each of which is arranged alternately with each of said first regions arranged along said first direction and each of which includes sub-word line drivers connected to said sub-word lines;

a plurality of third regions, each of which is arranged alternately with each of said first regions arranged along said second direction and each of which includes sense amplifiers connected to said data lines; and

a plurality of fourth regions, each of which is arranged alternately with each of said third regions arranged along said first direction,

wherein each of said plurality of main word lines extends through one or more of said first regions arranged along said first direction;

wherein said semiconductor memory further includes:

a plurality of pairs of sub-common data lines, each of which extends in said first direction through said third regions arranged along said first direction;

first switching circuits formed in said third regions and connected interposingly between said plurality of pairs of data lines and a corresponding one of said pairs of sub-common data lines;

a plurality of pairs of main-common data lines, each of which extends in said second direction through one or more of second regions arranged along said second direction; and

second switching circuits formed in said fourth regions and connected interposingly between a corresponding one of said pairs of main-common data lines and a corresponding one of said pairs of sub-common, data lines.

2. [A] The semiconductor according to claim 1,

wherein a number of memory arrays allotted to one of said main word-lines is greater than a number of memory arrays allotted to a corresponding one of said pairs of sub-common data lines.

3. [A] The semiconductor memory according to claim 1,

wherein a length of said each main word-line is longer than a length of said each pair of sub-common data lines.

5. [A] The semiconductor memory according to claim 4,

wherein said third region includes first sub-word line drivers coupled to said first sub-word lines and second sub-word line drivers coupled to said second sub-word lines.

6. [A] The semiconductor memory according to claim 4,

wherein each of said first and second sense amplifiers includes a pair of PMOS transistors and a pair of NMOS transistors, each of said pairs of PMOS and NMOS transistors having sources coupled in common, drains coupled to corresponding pairs of data lines and dates cross-coupled to said drains,

wherein each of said first and second sense amplifiers provides said corresponding pair of data lines with a pair of complementary signals having a high side voltage and a low side voltage on the basis of information of a corresponding one of said dynamic memory cells,

wherein, in a first period, said first and second sense amplifiers are driven by said first positive power supply voltage, and

wherein, in a second period following said first period, said first and second sense amplifiers are driven by said second positive power supply voltage.

8. [A] The semiconductor memory according to claim 7, wherein said semiconductor memory is formed on a P-type substrate comprising:

(1) a first N-well,

(2) a second N-well formed in said first N-well,

(3) a first P-well formed in said first N-well, and

(4) a second P-well formed in said first N-well,

wherein the source and the drain of said first PMOS are in said second N-well,

wherein the source and the drain of said first NMOS are in said first P-well, and

wherein the source and the drain of a switching NMOS transistor, forming one of said dynamic memory cells, are in said second P-well.

9. [A] The semiconductor memory according to claim 8, wherein said first N-well is supplied with a voltage corresponding to a high level of said first signal, and

wherein said P-type substrate is supplied with said ground potential.

10. A semiconductor memory comprising:

a plurality of first regions arranged in lattice fashion, each of which corresponds to a memory array including a plurality of main word lines extending in a first direction, a plurality of sets of sub-word lines extending in said first direction, a plurality of data lines extending in a second direction perpendicular to said first direction and a plurality of memory cells, each of which is coupled to a corresponding one of said plurality of sub-word lines and a corresponding one of said data lines, one of said plurality of main word lines being allotted to one of said plurality of sets of sub-word lines;

a plurality of second regions, each of which is arranged alternately with each of said first regions arranged along said second direction and each of which includes sub-word line drivers connected to said sub-word data lines;

a plurality of third regions, each of which is arranged alternately with each of said first regions arranged along said second direction and each of which includes sense amplifiers connected to said data lines; and

a plurality of fourth regions, each of which is arranged alternately with each of said third regions arranged along said first direction,

wherein each of said plurality of main word lines extends through one or more of said first regions arranged along said first direction,

wherein said semiconductor memory further includes:

a plurality of sub-common data lines, each of which extends in said first direction through said third regions arranged along said first direction;

first switching circuits connected interposingly between said plurality of data lines and said sub-common data lines;

a plurality of main-common data lines, each of which extends in said second direction through one or more of second regions arranged along said second direction; and

second switching circuits connected interposingly between said main-common data lines and said sub-common data lines.

11. The semiconductor memory according to claim 10,

wherein the number of memory arrays being allotted to one of main word-lines is greater than the number of memory arrays being allotted to one of said sub-common data lines.

12. The semiconductor memory according to claim 10,

wherein the length of said each main word-line is longer than the length of said sub-common data line.

wherein said third region includes first sub-word line drivers coupled to said first sub-word lines and second sub-word line drivers coupled to said second sub-word lines.

15. The semiconductor memory according to claim 13,

wherein each of said first and second sense amplifiers includes a pair of PMOS transistors and a pair of NMOS transistors, each of said pairs of PMOS and NMOS transistors having sources coupled in common, drains coupled to corresponding data lines and gates cross-coupled to said drains,

wherein said each of said first and second sense amplifiers provides corresponding data lines with signals having a high side voltage and a low side voltage on the basis of information of corresponding one of said dynamic memory cells.

wherein, in a first period, said first and second sense amplifiers are driven by said first positive power supply voltage, and

wherein, in a second period following said first period, said first and second sense amplifiers are driven by said second positive power supply voltage.

17. The semiconductor memory according to claim 16, wherein said semiconductor memory is formed on a P-type substrate comprising:

(1) a first N-well,

(2) a second N-well formed in said first N-well,

(3) a first P-well formed in said first N-well, and

(4) a second P-well formed in said first N-well,

wherein the source and the drain of said first PMOS are in said second N-well,

wherein the source and the drain of said first NMOS are in said first P-well, and

wherein the source and the drain of a switching NMOS transistor, forming one of said dynamic memory cells, are in said second P-well.

18. The semiconductor memory according to claim 17,

wherein said first N-well is supplied with a voltage corresponding to a high level of said first signal, and

wherein said P-type substrate is supplied with said ground potential.

19. A semiconductor memory comprising:

a plurality of word lines layered by main word lines and sub-word lines; and

a plurality of I/O lines layered by data lines connected to memory cells, sub-common data lines connected to said data lines and main-common data lines connected to said sub-common data lines,

wherein said main word lines, sub-word lines and sub-common data lines extend in a first direction, and

wherein said data lines and main-common data lines extend in a second direction perpendicular to said first direction.

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated November 26, 2002. Appreciation is expressed for the allowance of claims 4-9 and 14-18.